GaAs MMICs FOR DIGITAL RADIO FREQUENCY MEMORY (DRFM) SUBSYSTEMS

Gary K. Lewis, Inder J. Bahl and Edward L. Griffin
ITT Gallium Arsenide Technology Center
7670 Enon Drive, Roanoke, VA 24019
and
E. Ronald Schineller
ITT Avionics
500 Washington Avenue, Nutley, NJ 07110

ABSTRACT

A DRFM analog subsystem comprising of 10 GaAs MMIC chips (six limiting amplifiers, one quadrature IF downconverter, two IF amplifiers, and one quadrature upconverter) has been developed and integrated into an 11.8 cm^3 (.72 in^3) module. The input signal dynamic range for the module is 50 dB from 2-6 GHz, the image sideband rejection is 20 dB typical, and the LO to RF isolation is 27 dB minimum. The quadrature IF downconverter and quadrature upconverter in MMIC form are reported for the first time and operated as designed with good performance.

INTRODUCTION

A Digital RF Memory (DRFM) converts a microwave signal first to a baseband analog signal, then to a digital signal for storage in memory. It then formulates a digital response, reconstructs an analog signal, and upconverts the analog signal to the original microwave frequency. A block diagram of a typical DRFM is shown in Fig. 1. The MMIC module that we demonstrated comprises the key elements of the analog subsystem of a DRFM. It consists of a 50 dB gain limiting amplifier, a quadrature IF downconverter, a 20 dB gain IF amplifier for each IF channel, and a single sideband suppressed carrier upconverter. In Fig. 1 these components are indicated by solid line blocks. Note also that only one channel of the two quadrature channels is indicated in Fig. 1.

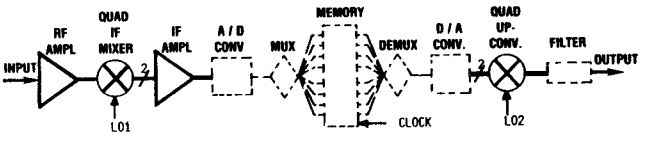

Figure 1 Block diagram of a Digital RF Memory. Analog circuits tested are indicated by solid line blocks.

FABRICATION PROCESS

The above mentioned circuits were fabricated using the standard ITT Gallium Arsenide Technology Center (ITT-GTC) microwave process for ion implanted GaAs. The active layer has a doping $n = 2x10^{17}$ cm^{-3} and thickness $t = .15$ μm. The process includes AuGe/Ni metallization for ohmic contacts, Ti/Pd/Au Schottky gates, Si_3N_4 overlay capacitors, and ion implanted resistors. The air bridges, microstrip lines, and bonding pads are 5 μm plated gold. The wafer is lapped to its final thickness of 125 μm; afterward backside via holes are etched and plated.

LIMITING AMPLIFIER

The limiting amplifier architecture shown in Fig. 2 consists of alternating diode limiter and linear amplifier stages cascaded such that the limiters restrict the signal to levels that enable the amplifiers to operate in a linear mode [1]. The amplifiers use resistive feedback to achieve low VSWRs and flat amplitude characteristics over a wide band. Each limiting amplifier IC has a small signal gain of 8.3 ± 0.5 dB and a VSWR < 2 at the input and the output. The second harmonic level is below -25 dBc. Figure 3 is a photograph of a single limiting amplifier chip.

Six limiting amplifier ICs were cascaded to create a 50 dB gain limiting amplifier module [2]. The output power is 12 dBm with a dc power supply of 4 Vdc at 500 mA. Figure 4 shows the measured performance of the limiting amplifier module. It can be seen that the output signals (Po) are nearly constant over the band for inputs (Pi) from -40 dBm to +10 dBm.

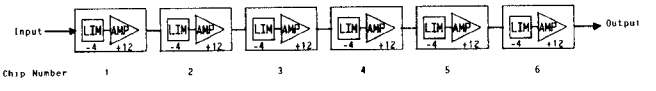

Figure 2 Six chip limiting amplifier configuration.

CH2478-6/87/0000-0053$01.00 © 1987 IEEE

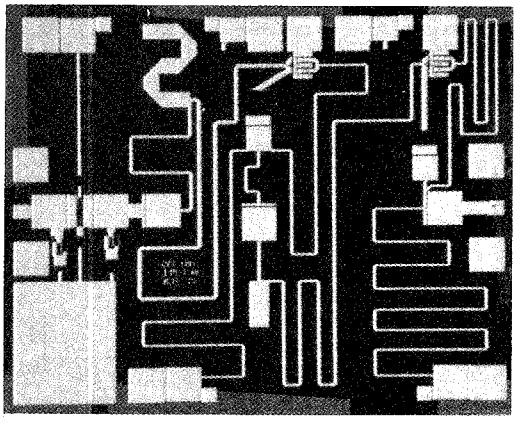

Figure 3 Photograph of a limiting amplifier chip. (Chip size: 3.8 mm x 3.0 mm)

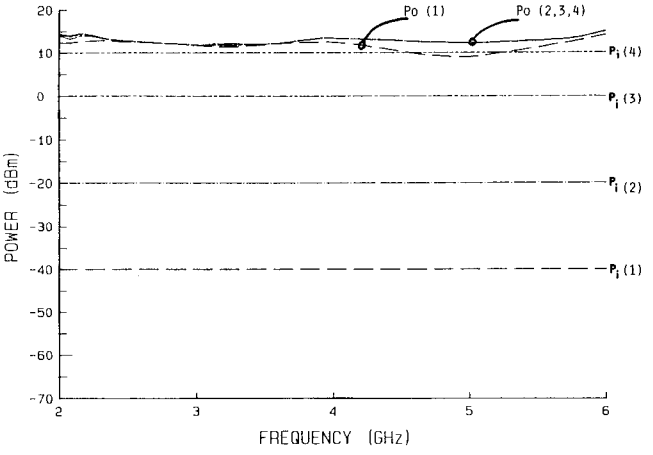

Figure 4 Output performance of a 6-stage limiting amplifier for several different input levels.

QUADRATURE IF DOWNCONVERTER

The quadrature IF downconverter provides two equal amplitude IF outputs that are in phase quadrature. The operating range is 2-6 GHz for the RF, 2.5-5.5 GHz for the LO, and 1 MHz-1 GHz for the IF. The downconverter is comprised of LO and RF power splitters and two mixers as shown in Fig. 5. The LO signal is fed to the two mixers through a quadrature 3 dB power divider (Lange coupler), and the RF signal is fed to the mixers via a two-section inphase power divider (Wilkinson power divider). The resultant IF output signals are in phase quadrature and of equal amplitude. The phase of one IF output signal leads or lags the other signal depending on whether the RF frequency is greater or less than the LO frequency.

The IF output signals are required to amplitude and phase track in this application so that when the two IF signals are upconverted the unwanted sideband is suppressed. To ensure IF tracking distributed FET mixers [3,4] were chosen for this circuit because they provide good matched wideband characteristics when they are integrated on the same chip.

The distributed dual-gate FET mixer design was based on small signal analysis. FET S parameters were taken with dual-gate FETs biased at the point where the conversion gain was measured to be maximum (-5 dB) with I_{ds} constrained to be about 10 mA. Using the three-port S-parameter data a dual-gate FET model was synthesized, and then a distributed amplifier having 4 cells was designed for maximum gain flatness from 1 MHz to 7 GHz. The computed gain of the distributed amplifier was -2.4 ± 0.3 dB. Adding the power dividers to the amplifier, the computed gain of the entire downconverter (without the diplexer) was -6.5 ± .5 dB in the 1-7 GHz band. The maximum computed output amplitude difference was .5 dB and the maximum computed phase difference was 3 degrees.

A diplexer was added at the output of each mixer circuit to provide a 50 ohm load and good LO to IF isolation. The diplexer was designed to have a crossover frequency of 1.5 GHz and to give 30 dB suppression to signals whose frequency was greater than 2 GHz.

A photograph of the quadrature IF downconverter is shown in Fig. 6. The IC was tested with an RF input from 2 to 6 GHz; a typical measurement of amplitude tracking for the two output channels is shown in Fig. 7. The amplitude and phase tracking performance between the two IF channels was typically better than ± 0.5 dB and ± 5 degrees, respectively. The design goals were ± 0.5 dB and ± 5 degrees maximum. The measured conversion loss was 9 dB.

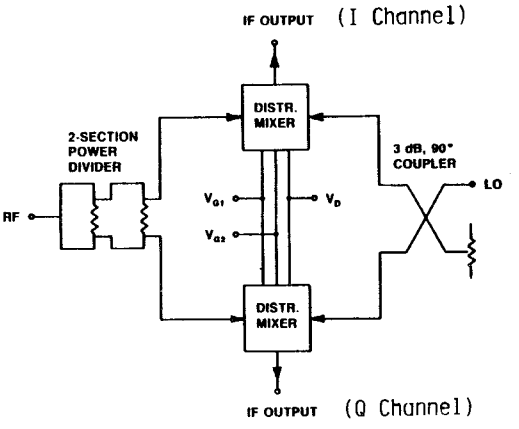

Figure 5 Quadrature IF downconverter configuration.

IF AMPLIFIER

The IF amplifier was designed to operate from

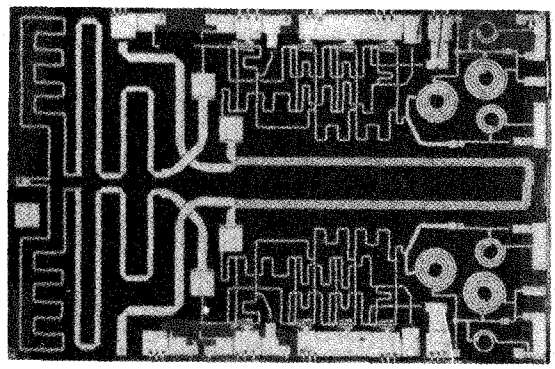

Figure 6 Photograph of a quadrature IF downconverter. (Chip Size: 5.9 x 3.8 mm)

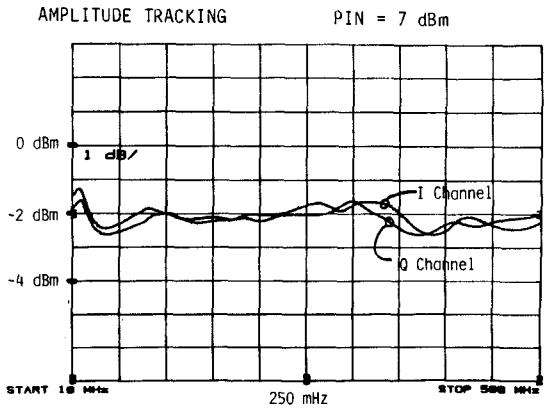

Figure 7 Measured outputs from a quadrature IF downconverter.

0.1 to 2.0 GHz. The IC consists of two stages with feedback in the first stage. Figures 8 and 9 show the photograph, and the measured and calculated performance of the IF amplifier, respectively. Note that the agreement between the calculated and measured performance is good. The chip has 20 dB gain and input and output VSWRs of < 2.0. The measured 1 dB compression point was 13 dBm and the noise figure was 3.5 dB.

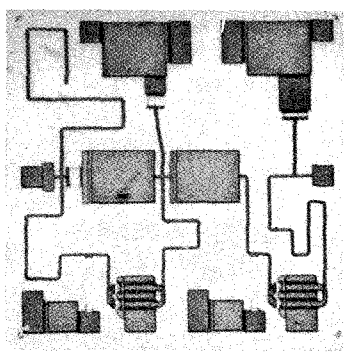

Figure 8 Photograph of an IF amplifier. (Chip Size: 1.7 x 1.7 mm)

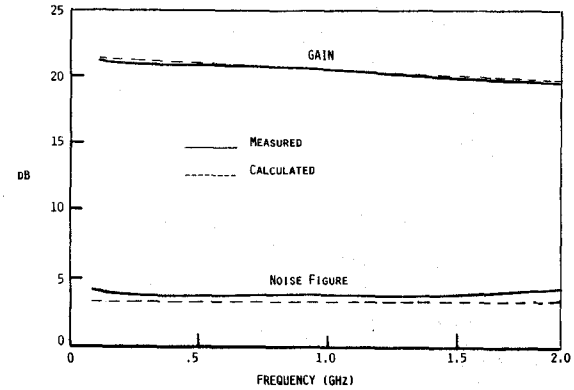

Figure 9 Measured and calculated response of an IF amplifier.

QUADRATURE UPCONVERTER

The single sideband suppressed carrier upconverter is comprised of LO and RF power splitters, IF/RF diplexers, and the two single balanced mixers (Fig. 10). The balanced mixers were designed using Schottky diodes. The LO signal is fed to the two balanced mixers via an inphase 3 dB power divider, and the quadrature IF signals are fed to the mixers from the IF amplifiers thru on-chip diplexers. The resultant output RF signals (LO ± IF) from the two balanced mixers are summed in a quadrature (Lange) coupler. For quadrature phase IF inputs the summing process enhances the signal level of one sideband signal and suppresses the other sideband signal. The operating frequency range for the mixers is 1 MHz to 1 GHz at the IF ports, 7 GHz for the LO signal, and 6 to 8 GHz for the RF output signals. In a complete DRFM, a second mixer would be used to convert the output signal back to the original input frequency. Figure 11 shows the photograph of the quadrature upconverter. The output spectrum of the IC with a 1 GHz IF input signal is shown in Fig. 12.

The design goals for these circuits were to have the unwanted sideband suppressed > 25 dB and LO to IF isolation > 30 dB, whereas, the measured performance of the quadrature upconverter was 25 dB and 27 dB, respectively.

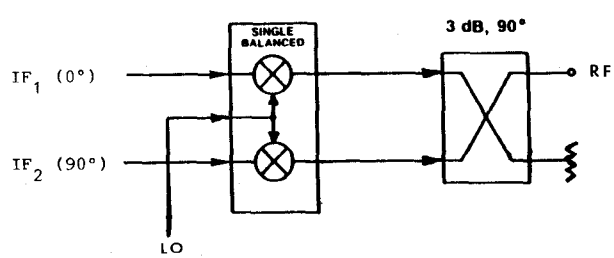

Figure 10 Quadrature Upconverter Configuration.

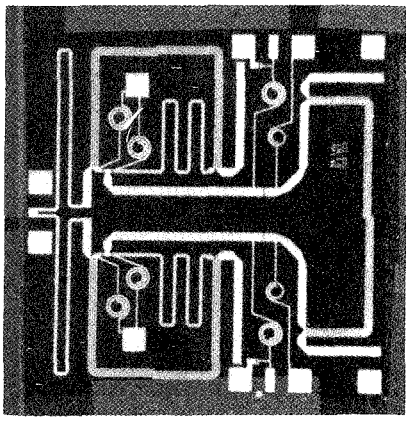

Figure 11 Photograph of a quadrature upconverter. (Chip Size: 4.0 x 4.0 mm).

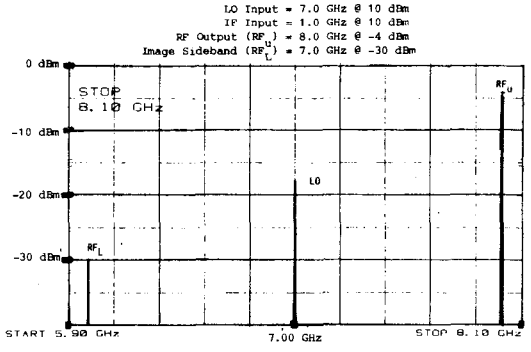

Figure 12 Measured output spectrum of an upconverter.

DRFM MODULE

The DRFM module (Fig. 13) contains three drop-in carriers that have been pretested. The first two carriers contain 3 limiting amplifier ICs each. The third carrier contains four ICs; a quadrature downconverter, two IF amplifiers, and an upconverter. DC bypass capacitors and bias lines are contained on the individual carriers and in the DRFM module.

Figure 14 shows a measured output spectrum of the module. The image sideband (RF_L) suppression is 20 dB typical, and the LO to IF isolation is 27 dB minimum; the design goals were 25 dB and 30 dB, respectively. The VSWR at all ports (input, LO1, LO2, and output) is better than 2.0:1.

CONCLUSION

An analog subsystem of a DRFM has been developed. It has been shown that a MMIC based DRFM subsystem can be built which has near state-of-the-art performance. In production the assembly time will be much less than that for a hybrid based subassembly because there are far fewer components to assemble and considerably fewer interconnections. The test time will also be less because an on-wafer probe station can be used to preselect good ICs and there is no subassembly tuning. These features imply subsystem cost reductions.

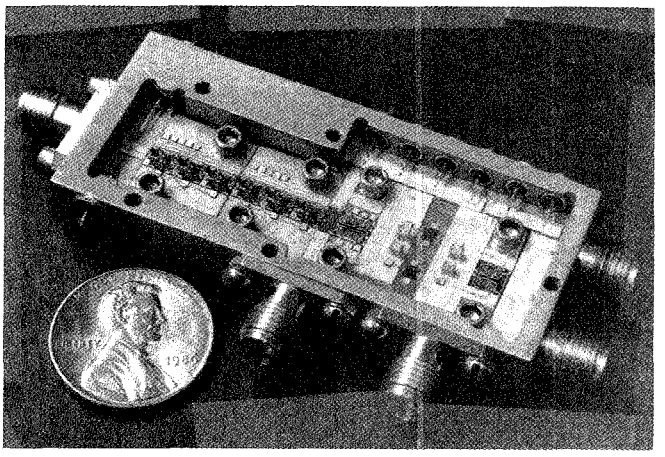

Figure 13 Photograph of the DRFM analog subsystem.

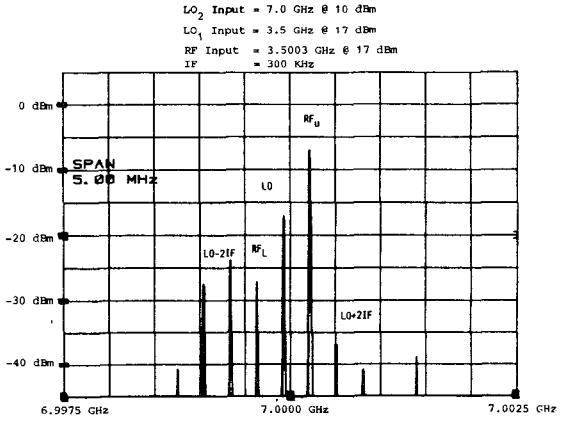

Figure 14 Measured output spectrum of the DRFM analog subsystem.

ACKNOWLEDGEMENTS

The authors gratefully acknowledge the assistance of many colleagues at ITT-GTC and ITT-Avionics, including the layout, fabrication, quality control, packaging, and microwave test groups.

REFERENCES

[1] E. J. Crescenzi, Jr., et al, "Wide-Band Limiting Amplifier with Low Second Harmonic Distortion, Utilizing GaAs MMIC Limiters", IEEE MTT-S Digest, 1985, pp. 328-331.

[2] I. Bahl, E. Griffin, and R. Schineller, "GaAs Monolithic Limiting Amplifiers", GaAs IC Symp. Digest, Oct. 1986, pp. 71-73.

[4] O. Tang and C. Aitchison, "A Very Wide-Band Microwave MESFET Mixer Using The Distributed Mixing Principle", IEEE Trans Microwave Theory, Vol. MTT-33, Dec. 1985, pp. 1470-1478.

[5] T. Howard and A. Pavio, "A Distributed 1-12 GHz Dual-Gate FET Mixer", IEEE MTT-S Digest, 1986, pp. 329-332.